**After Midterm Assignment1**

1) Show MIPS **single cycledata path** for the following *load* instruction set (where **S0** and **S1** are 32-bit general purpose registers and S0 has initialized with a value of zero):

 **lw S1, 8(S0)**

2) Consider the following MIPS assembly code (where S0, S1, and S6 are 32-bit general purpose registers, and S0 has initialized with a value of zero):

 i) **addi S0, S0,5**

ii) **lw S6, 5(S0)**

 iii) **addi S0, S0,3**

iv) **sw S1, 7(S0)**

 2.1) [2 Points] Show the **immediate values** (in hexadecimal) in register **S0** after the execution of the instruction (i) and (iii).

 2.2) [3 Points] Show the **32-bit physical memory addresses** (in hexadecimal) of the instructions (ii), and (iv).

3) Consider the following MIPS assembly code (where S0, S1, and S2 are 32-bit general purpose registers, and S0 has initialized with a value of zero):

 i) **addi S0, S0,7**

ii) **sw S1, 8(S0)**

 iii) **addi S0, S0,4**

iv) **lw S2, 4(S0)**

 3.1) [2 point] Show the **immediate value** (in hexadecimal) in register **S0** after the execution of the instruction (i) and (iii).

 3.2) [3 points] Show the **32-bit physical memory addresses** (in hexadecimal) of the instructions (ii), and (iv).

4) Consider the following MIPS instruction (where S0 and S1 are two 32-bit general purpose integer registers):

**lw S1, 0x11(S0)**

Assume that the register **S0** has initialized with a value of zero. Show the value of the register **S1** after the *load* operation based on the data memory which is shown in Figure 1.



Figure 1.

5) Assume that a compiler (C/C++/Java) which is running on a MIPS system generates the following assembly code (where S0, S1, S2, S3, and S4 are 32-bit general purpose registers). Show its **equivalent high level code**.

**beq S3, S4, L1**

**add S0, S1, S2**

**j L2**

**L1:**

**sub S0, S0, S3**

**L2:**

6) Consider the following *store* instruction (where S0 and S1 are two 32-bit general purpose integer registers):

 **sw S1, 15(S0)**

Assume that S0 is initialized with a value of zero and S1 has a 32-bit number, **0xFF223344**. Show the **byte addressable** **memory** of the MIPS system after the execution of the store instruction.

7) Consider memory storage of a **32-bit word** stored at memory **word 4** in a byte-addressable memory.

7.1) [1 point] What is the byte address of memory word 4?

7.2) [1 point] What are the byte addresses that memory word 4

 spans?

7.3) [3 points] Draw the number 0xFF223344 stored at word 4 in both **big-endian** and **little-endian** machines (your drawing should clearly label the byte address corresponding to each data byte value).