**After midterm – Assignment 2**

1) Single cycle MIPS system is pipelined by subdividing its *data path* into *five pipeline stages*. Briefly describe the **pipeline stages** of the processor.

2) The pipelined MIPS processor is running the following program. Which registers are being *written*, and which are being *read* on the **sixth cycle** (where S1, S2, S3, S4, T0, T1, T2, T3 and T4 are 32-bit general purpose registers)?addi S1, S2,5

 sub T0, T1, T2

 lw T3, 15(S1)

 sw T4, 72(T0)

 Or T2, S3, S4

3) Using a **pipeline sequence diagram**, show the *forwarding* and *stalls* needed to execute the following instructions on the pipelined MIPS system (where S1, S2, S3, S4, S5, S6, S7, S8 and S9 are 32-bit general purpose registers).

lw S6, 10(S5)

and S3, S6, S7

or S2, S6, S9

add S1, S2, S3

sub S4, S1, S5

xor S10, S3, S1

4) Using a **pipeline sequence diagram**, show the *forwarding* and *stalls* needed to execute the following instructions on the pipelined MIPS system (where S0, S1, S2, S3, S4, S5, S6, S7, S8 and S9 are 32-bit general purpose registers).

addi S1, S0, 5

add S4, S1, S5

xor S10, S3, S4

lw S6, 8(S5)

or S3, S6, S7

and S2, S6, S9

5) Describe the term ***structural hazard*** in a pipeline system. How the MIPS system solve the problem with **register file** read and write operation in 1 clock cycle during its pipeline instruction execution.

6) Consider an **un-pipelined** machine with five stages (Instruction Fetch, Instruction Decode/Register Fetch, Execute/Address Calculation, Memory Access and Write Back). Assume that it has **1ns** clock cycles. The machine uses four cycles for ALU operations and branches and five cycles for memory operations. Assume that the relative frequencies of these operations are 45%, 15% and 40% respectively. **Pipelining the machine** adds **1.2 ns** of overhead to the clock. Find out how much **speedup** we will gain in the instruction execution rate. You can ignore any latency impact.

7) Consider a **2MB** cache (assume that there is no level2 cache in the system) and a **4GB** main memory (organization: 2G x 16). If the size of a main memory block is 128-bit (**eight**, 16-bit words), then show the address fields which are used by a processor to access the following cache organizations;

 7.1) *Direct*

 7.2) *Fully associative*

 7.3) 2-*way set associative*

8) Consider a **4MB** cache (assume that there is no level2 cache in the system) and a **2GB** main memory (organization: 2G x 8). The size of a main memory block is 64-bit (**eight**, 8-bit words). Based on the given cache, memory block and main memory details show the address fields which are used by a processor to access the following cache organizations:

 8.1) *Direct*

 8.2) *Fully associative*

 8.3) 4-*way set associative*

9) Consider a **4MB** cache (assume that there is no level2 cache in the system) and a **4GB** main memory (organization: 2G x 16). The size of a main memory block is 128-bit (**eight**, 16-bit words). Assume that the processor can only access a word of 16-bit at time from the cache. Based on the given cache, memory block, and main memory details show the address fields which are used by a processor to access the following cache organizations:

 9.1) *Direct*

 9.2) *Fully associative*

 9.3) 4*-way set associative*

10) Discuss briefly cache **read** and **write** policies.

11) Assume that the hit time of a 2-*way set-associative* L1 data cache is 1.5 times faster than a 4-*way set-associative* cache of the same size. The miss rate of 2-way cache is 0.049 and 4-way is 0.044 (for an 8KB data cache). Assume a hit is 1 clock cycle. Assume the miss penalty is 10 clock cycles for the 2-way set-associative cache, and the miss penalty of 4-way is 2 clocks less than 2-way cache. Calculate their **AMATs** (Average Memory Access Time).