**Lecture 02 Assignments**

**Combinational Logic**

1) Consider the following truth table (where *A*, *B*, and *C* are 3 input variables and *Y* is an output variable):

|  |  |  |  |
| --- | --- | --- | --- |
| ***A*** | ***B*** | ***C*** | ***Y*** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

 1.1) Write a Boolean equation in *sum-of-products* canonical form.

 1.2) Minimize the equation from **1.1** using a ***K-map*** and sketch its combinational logic circuit.

2) Consider the following truth table (where *A*, *B*, and *C* are 3 input variables and *Y* is an output variable):

|  |  |  |  |
| --- | --- | --- | --- |
| ***A*** | ***B*** | ***C*** | ***Y*** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

 2.1) Write a Boolean equation in *sum-of-products* canonical form.

2.2) Minimize the equation from **2.1** using a ***K-map*** and sketch its combinational circuit.

3) Create the following logic functions using NAND gate(s):

 3.1) a two-input AND

 3.2) a two-input NOR

 3.3) a two-input OR

 3.4) a two-input XOR

4) Simplify the following logic equations and *sketch the circuits*:

 4.1) *Y* = 

 4.2) *Y* = 

 4.3) *Y* =

 4.4) *Y* =

5) Create the circuit schematic of a **4-line Multiplexer** using its truth table.

 6) Create a 4-bit *parity checker* using XOR gates.

7) Create the circuit schematic of a **4-line Decoder** using its truth table. Show the address ranges which are used to select **four** memory chips (each with size **16K × 8**) by the decoder.